تکلیف طراحی آپ امپ:

Design and simulate a single-ended two-stage OTA with PMOS input differential pair and NMOS second stage to meet the following specifications:

V_{DD}=1.8V
Load Capacitance: 3 pF
DC Gain > 1000
f_{ta}> 300 MHz
PM > 65^o for β=1
Input CM range: At least 0.5 V to 0.9V
Output swing (peak-to-peak)> 1.4Vpp
Power dissipation: ***As low as possible***

1-Estimate required MOS parameters (such as $\mu_n C_{ox}$ and λ) by simulating single NMOS and PMOS transistors.
2-Use basic equations and your knowledge to have a staring design point (W/L and current of transistors, C_C and R_Z). ***describe your design flow***.

3-Implement your design in the 0.18um technology in the TT-27^{o}C corner case. If the results are far from the required specifications, optimize the circuit. ***describe your optimization flow***

4-For the designed OTA, simulate the frequency response (phase and magnitude) and show DC gain, PM, and f_T. Prove that your OTA works in the input CM and output swing range by proper simulations.

5-Chage corners to SS 120 and FF -40. Repeat part 4 again. Modify your circuit if necessary to make sure tour design meet the specs.